Fig. 1 PRIOR ART

XADD

ICLK

YADD2

17

LATCH CIRCUIT

LATCH CIRCUIT

18

ARAS

12

XE

ROW ADDRESS DECODER

SE

11

13

10

WL

BL

COLUMN ADDRESS DECODER

MEMORY CELL ARRAY

SENSE AMPLIFIER

14

15

RO

WI
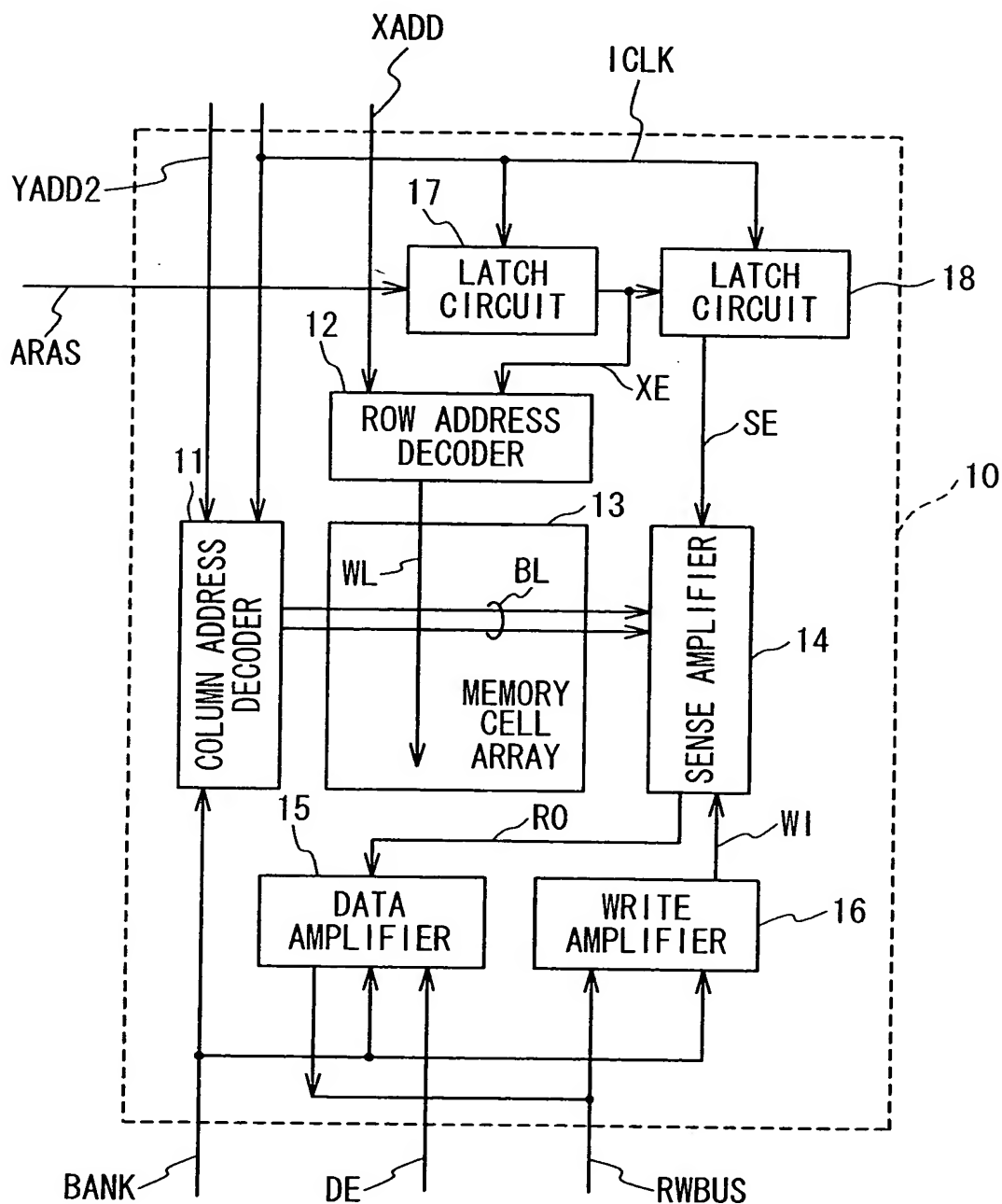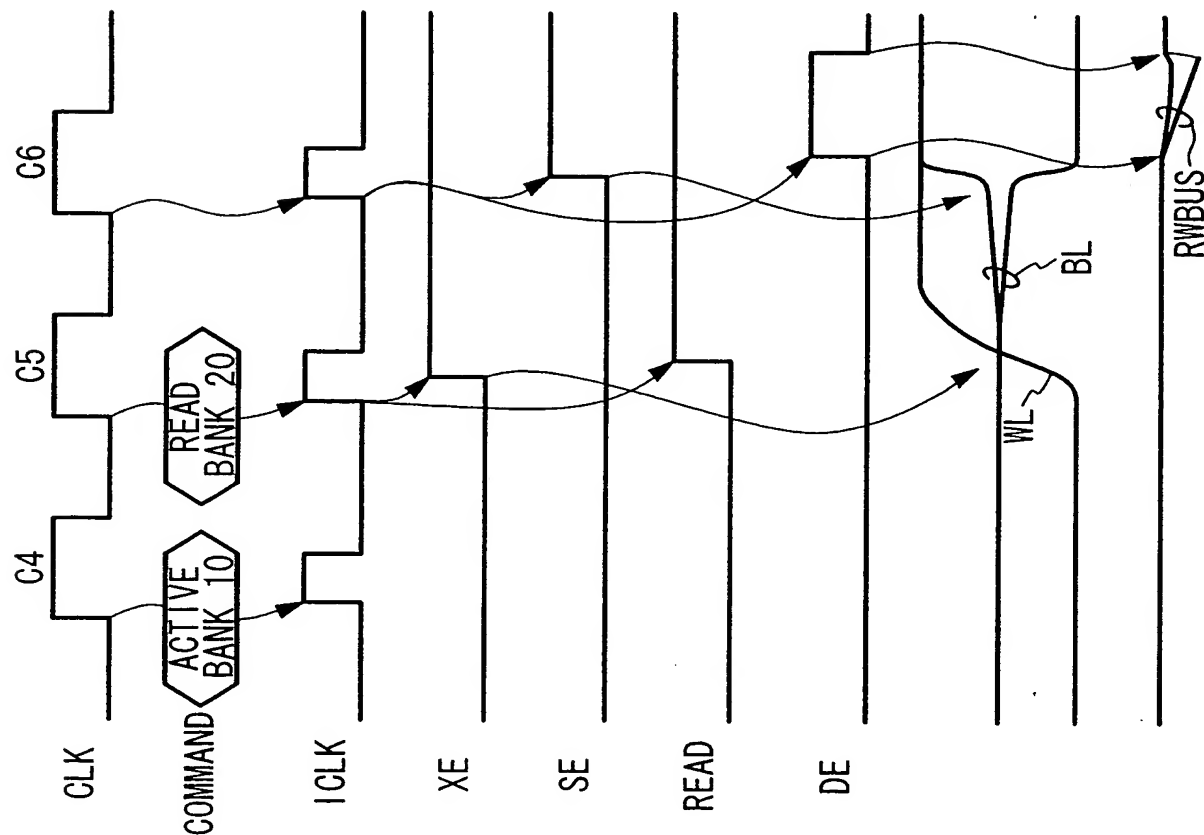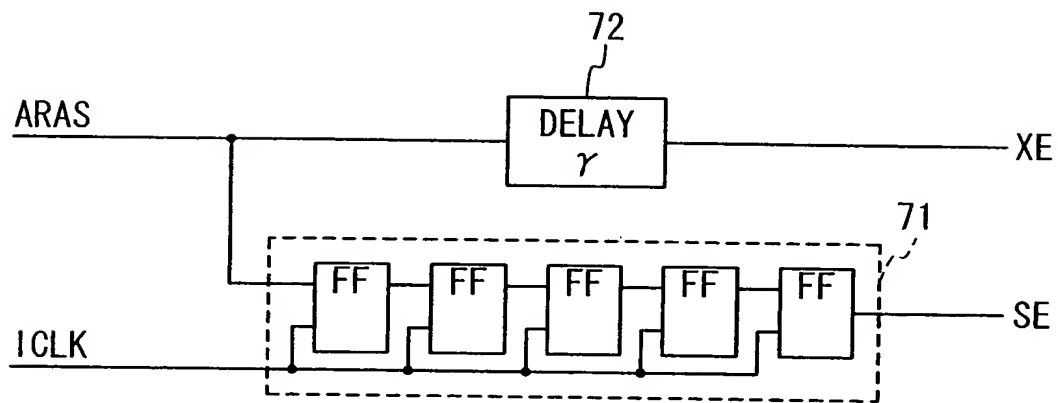
DATA AMPLIFIER

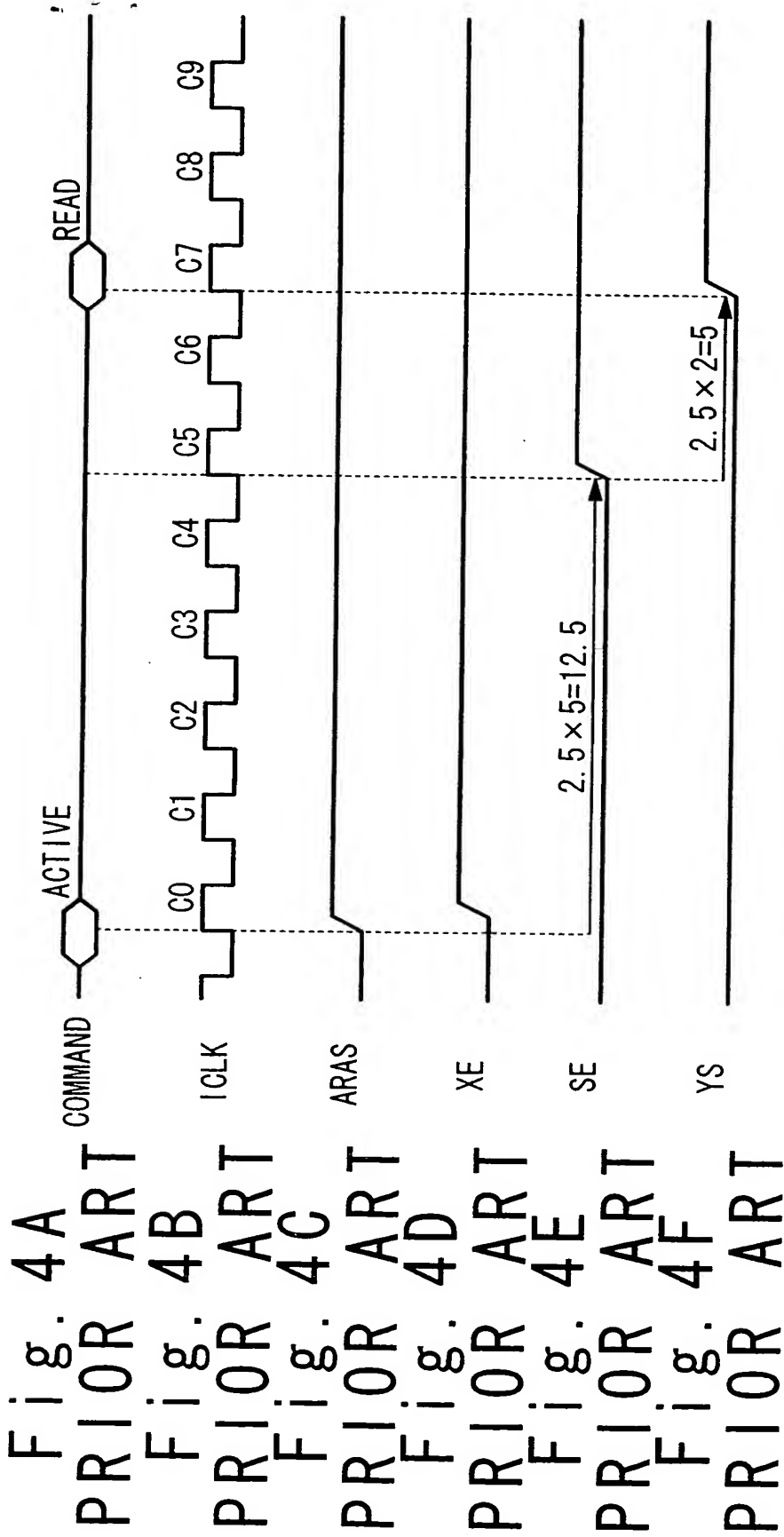WRITE AMPLIFIER

16

BANK

DE

RWBUS

Fig. 2A PRIOR ART
Fig. 2B PRIOR ART
Fig. 2C PRIOR ART
Fig. 2D PRIOR ART
Fig. 2E PRIOR ART
Fig. 2F PRIOR ART
Fig. 2G PRIOR ART
Fig. 2H PRIOR ART
Fig. 2I PRIOR ART
Fig. 2J PRIOR ART

Fig. 3 PRIOR ART

ARAS

72

DELAY
γ

XE

71

FF FF FF FF FF

ICLK

SE

Fig. 4A PRIOR ART COMMAND

Fig. 4B PRIOR ART ICLK

Fig. 4C PRIOR ART ARAS

Fig. 4D PRIOR ART XE

Fig. 4E PRIOR ART SE

Fig. 4F PRIOR ART YS

Fig. 5A
PRIOR ART

Fig. 5B
PRIOR ART

Fig. 5C
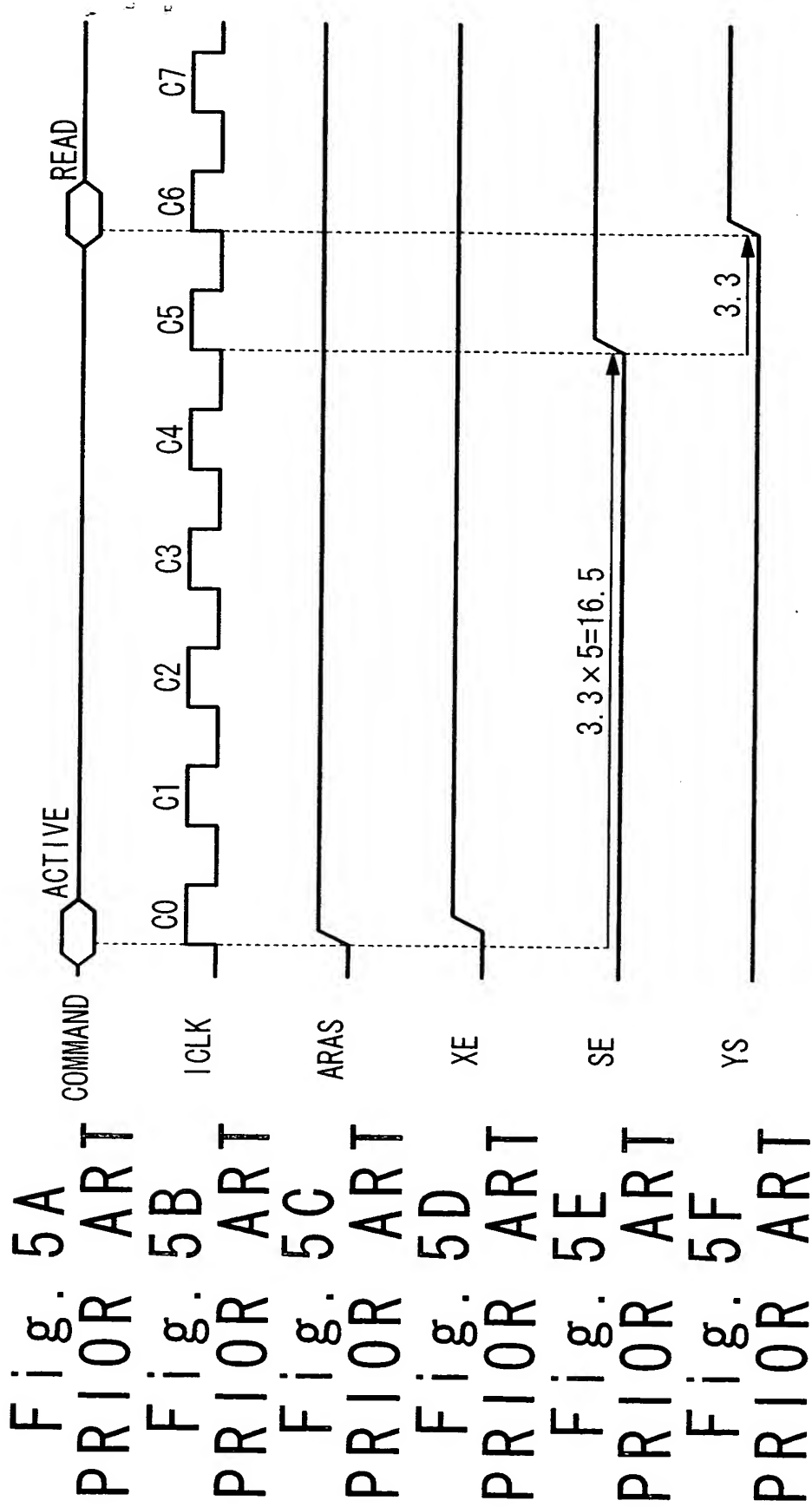PRIOR ART

Fig. 5D
PRIOR ART

Fig. 5E
PRIOR ART
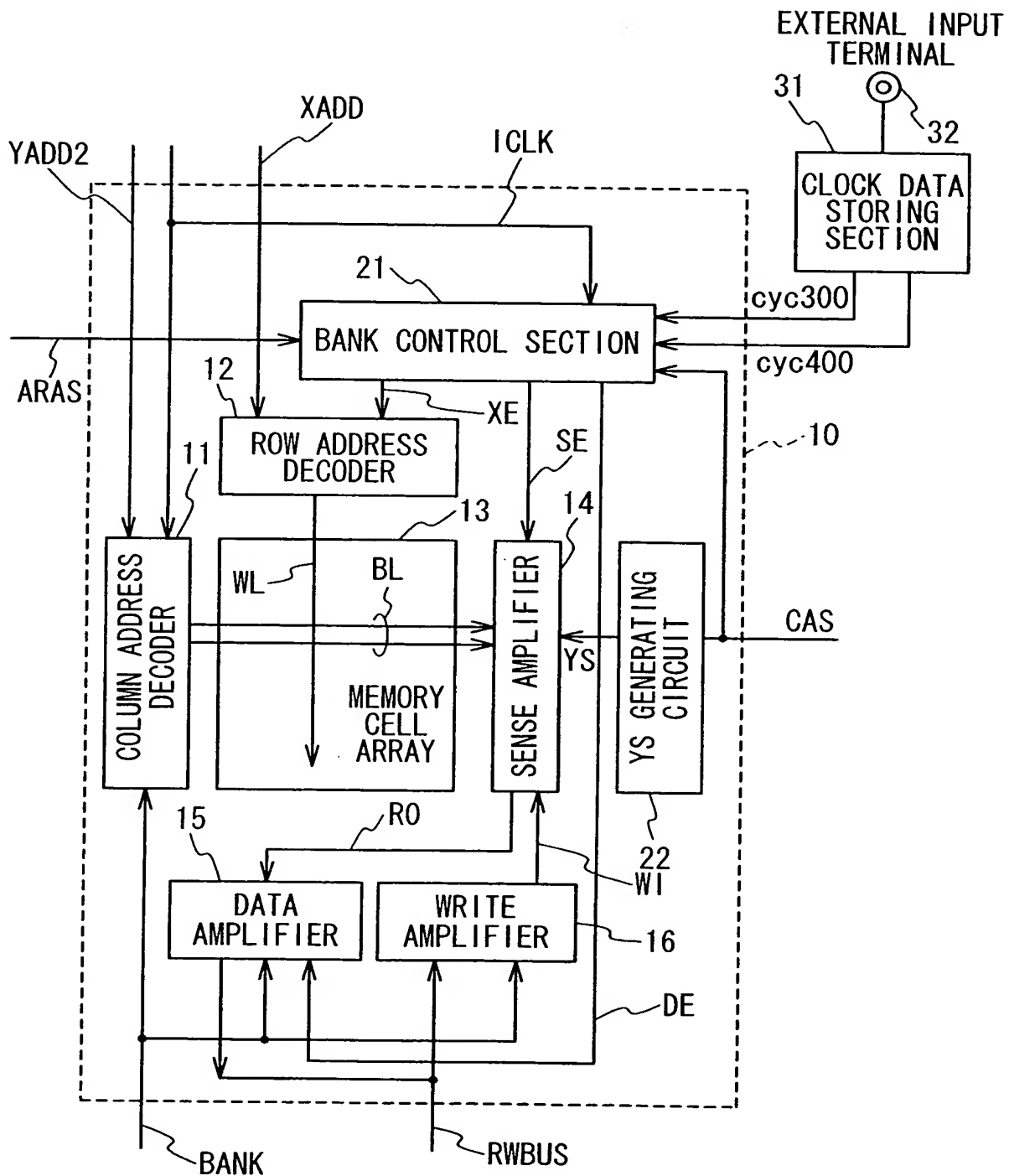
Fig. 5F
PRIOR ART

COMMAND

ICLK

ARAS

XE

SE

YS

ACTIVE

READ

C0 C1 C2 C3 C4 C5 C6 C7

$3.3 \times 5 = 16.5$

3.3

Fig. 6

Fig. 7

Fig. 8A COMMAND

Fig. 8B ICLK

Fig. 8C ARAS

Fig. 8D XE

Fig. 8E SE

Fig. 8F CAS

Fig. 8G YS

Fig. 8H DE

Fig. 9 A COMMAND

Fig. 9 B ICLK

Fig. 9 C ARAS

Fig. 9 D XE

Fig. 9 E SE

Fig. 9 F CAS

Fig. 9 G YS

Fig. 9 H DE

ACTIVE

READ

C0 C1 C2 C3 C4 C5 C6 C7 C8

$3.3 \times 3.5 + \alpha = 12.5$

$\pm \alpha$

$8.25 - \alpha = 7.4$

$3.3 \times 2 = 6.6$